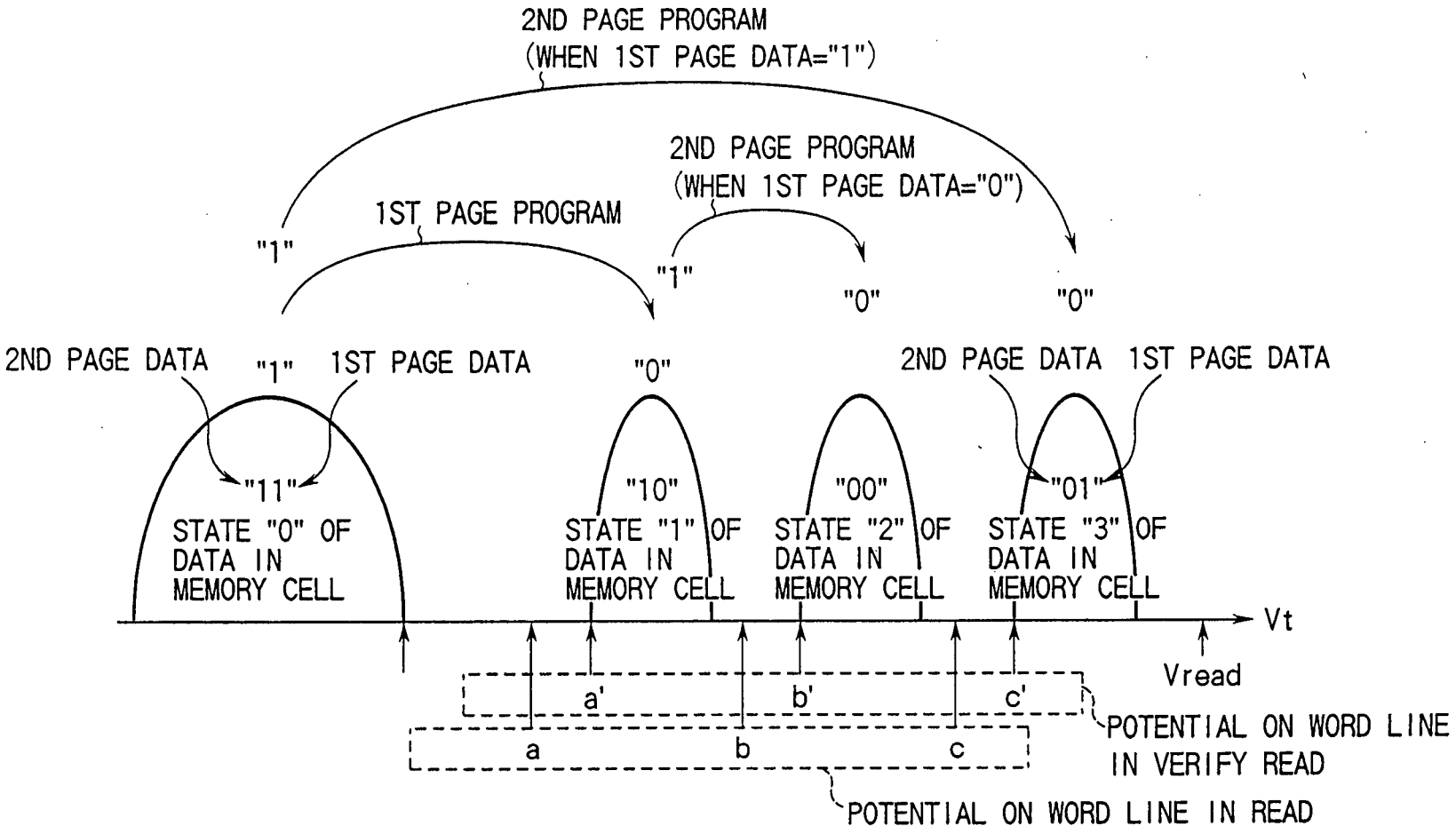
2ND PAGE PROGRAM
(WHEN 1ST PAGE DATA="1")
2ND PAGE PROGRAM
(WHEN 1ST PAGE DATA="0")
1ST PAGE PROGRAM
"1"
"1"
"0"
"0"
2ND PAGE DATA
"1"
1ST PAGE DATA
"0"
2ND PAGE DATA
1ST PAGE DATA
"11"
"10"
"00"
"01"
STATE "0" OF DATA IN MEMORY CELL
STATE "1" OF DATA IN MEMORY CELL
STATE "2" OF DATA IN MEMORY CELL
STATE "3" OF DATA IN MEMORY CELL
Vt
Vread
a'
b'
c'
a
b
c
POTENTIAL ON WORD LINE IN VERIFY READ
POTENTIAL ON WORD LINE IN READ

FIG. 1

DATA (STATE) IN MEMORY CELL	THRESHOLD VOLTAGE OF MEMORY CELL	DATA TO BE WRITTEN AND READ	
		2ND PAGE	1ST PAGE
0	0V OR BELOW	1	1
1	0.3V~0.5V	1	0
2	0.8V~1.0V	0	0
3	1.3V~1.5V	0	1

FIG. 2

DATA (STATE) IN MEMORY CELL	THRESHOLD VOLTAGE OF MEMORY CELL	DATA TO BE WRITTEN AND READ	
		2ND PAGE	1ST PAGE
0	0V OR BELOW	1	1
1	0.3V~0.5V	1	0
2	0.8V~1.0V	0	1
3	1.3V~1.5V	0	0

FIG. 3

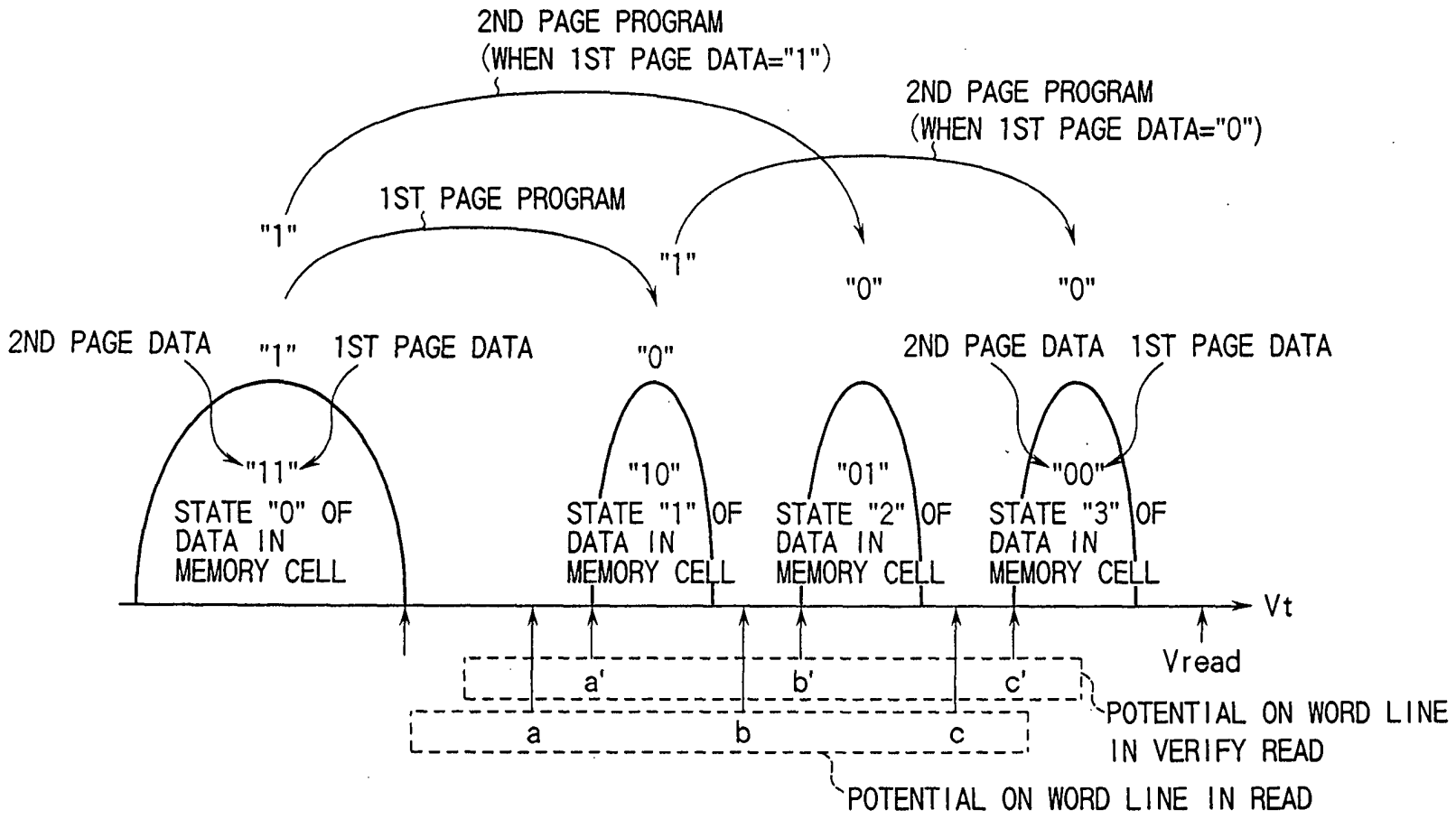
2ND PAGE PROGRAM
(WHEN 1ST PAGE DATA="1")
2ND PAGE PROGRAM
(WHEN 1ST PAGE DATA="0")
1ST PAGE PROGRAM
"1"
"1"
"0"
"0"
2ND PAGE DATA
"1"
1ST PAGE DATA
"0"
2ND PAGE DATA
1ST PAGE DATA
"11"
"10"
"01"
"00"
STATE "0" OF DATA IN MEMORY CELL
STATE "1" OF DATA IN MEMORY CELL
STATE "2" OF DATA IN MEMORY CELL
STATE "3" OF DATA IN MEMORY CELL
Vt
Vread
a'
b'
c'
a
b
c
POTENTIAL ON WORD LINE IN VERIFY READ
POTENTIAL ON WORD LINE IN READ

FIG. 4

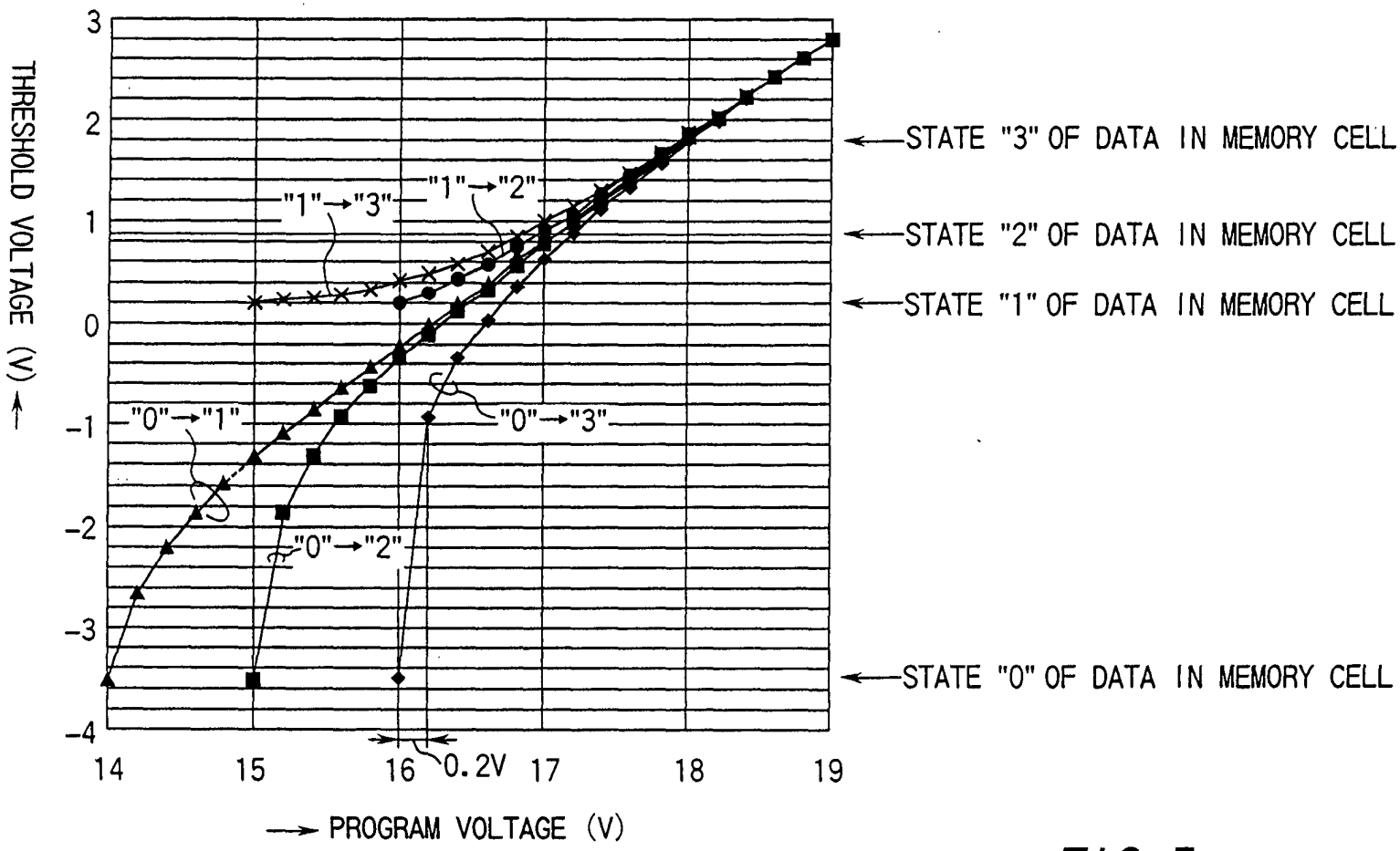
THRESHOLD VOLTAGE (V)
3
2
1
0
-1
-2
-3
-4
14
15
16
0.2V
17
18
19
PROGRAM VOLTAGE (V)
"1"→"3"
"1"→"2"
"0"→"1"
"0"→"3"
"0"→"2"
STATE "3" OF DATA IN MEMORY CELL
STATE "2" OF DATA IN MEMORY CELL
STATE "1" OF DATA IN MEMORY CELL
STATE "0" OF DATA IN MEMORY CELL

FIG. 5

EXAMPLE OF FIG. 3	NO. OF NECESSARY STEP-UPS	
1ST PAGE WRITING	13	(0→1)13
2ND PAGE WRITING	16	(0→2)13 (1→3)16
TOTAL	29	

FIG. 6

PRESENT INVENTION	NO. OF NECESSARY STEP-UPS	
1ST PAGE WRITING	13	(0→1)13
2ND PAGE WRITING	11	(0→3)11 (1→2)6
TOTAL	24	

FIG. 7

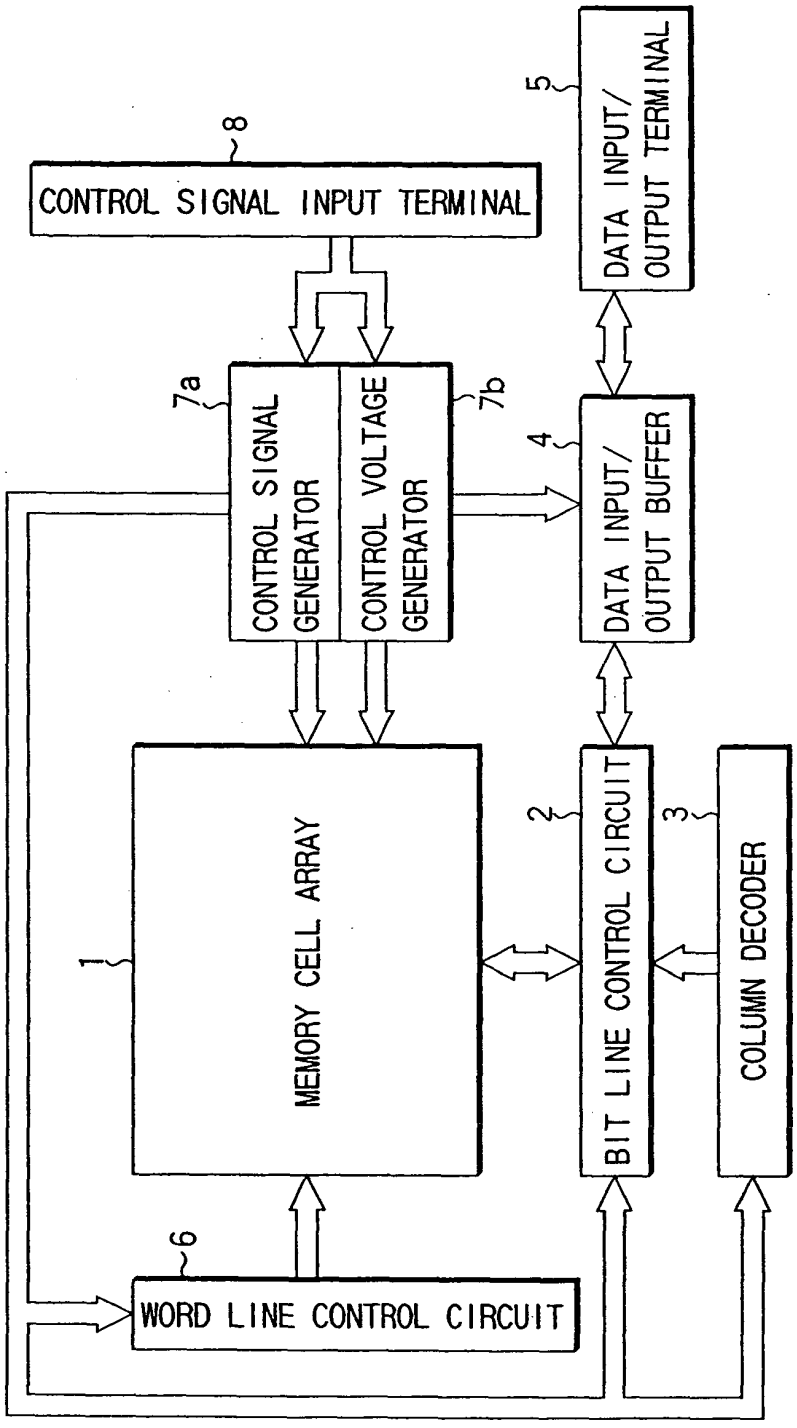
8
CONTROL SIGNAL INPUT TERMINAL
5
DATA INPUT/
OUTPUT TERMINAL
7a
CONTROL SIGNAL
GENERATOR
7b
CONTROL VOLTAGE
GENERATOR
4
DATA INPUT/
OUTPUT BUFFER
1
MEMORY CELL ARRAY
2
BIT LINE CONTROL CIRCUIT
3
COLUMN DECODER
6
WORD LINE CONTROL CIRCUIT

FIG. 8

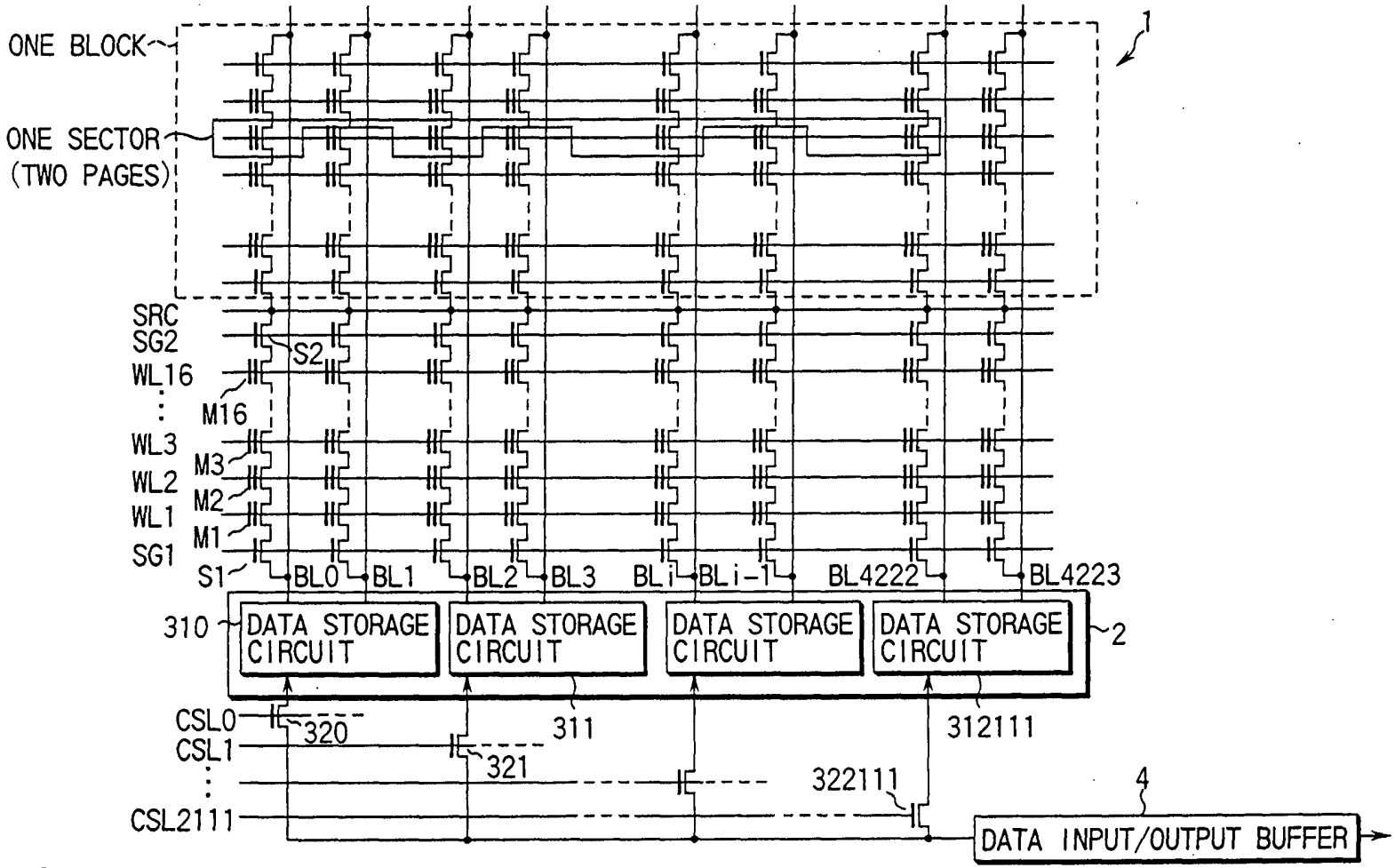
ONE BLOCK
ONE SECTOR
(TWO PAGES)
1
SRC
SG2
WL16
M16
WL3
M3
WL2
M2
WL1
M1
SG1
S1
S2
BL0
BL1
BL2
BL3
BLi
BLi-1
BL4222
BL4223
310
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT
2
CSL0
CSL1
CSL2111
320
321
311
312111
322111
4
DATA INPUT/OUTPUT BUFFER

FIG. 9

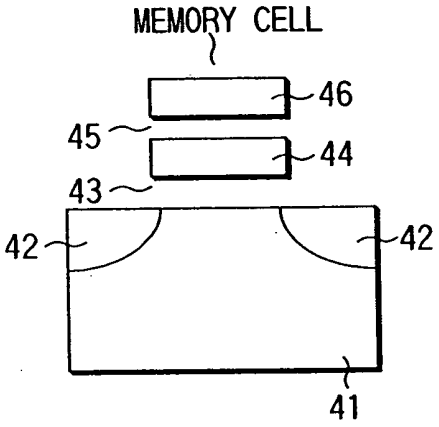

FIG. 10A

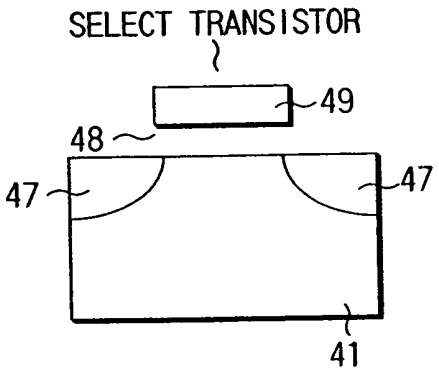

FIG. 10B

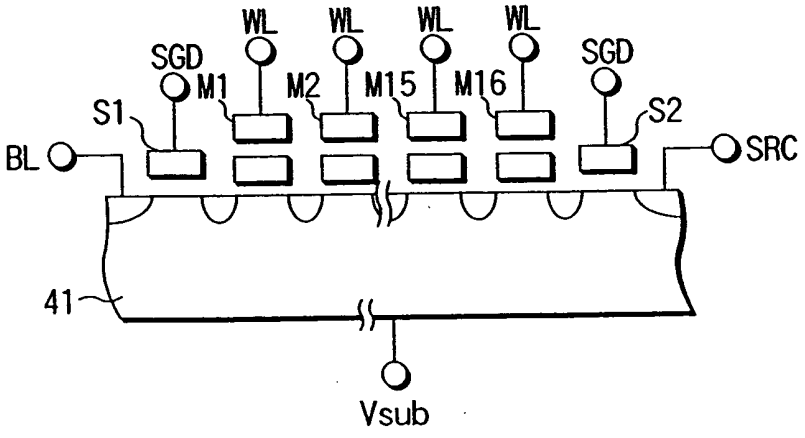

FIG. 11

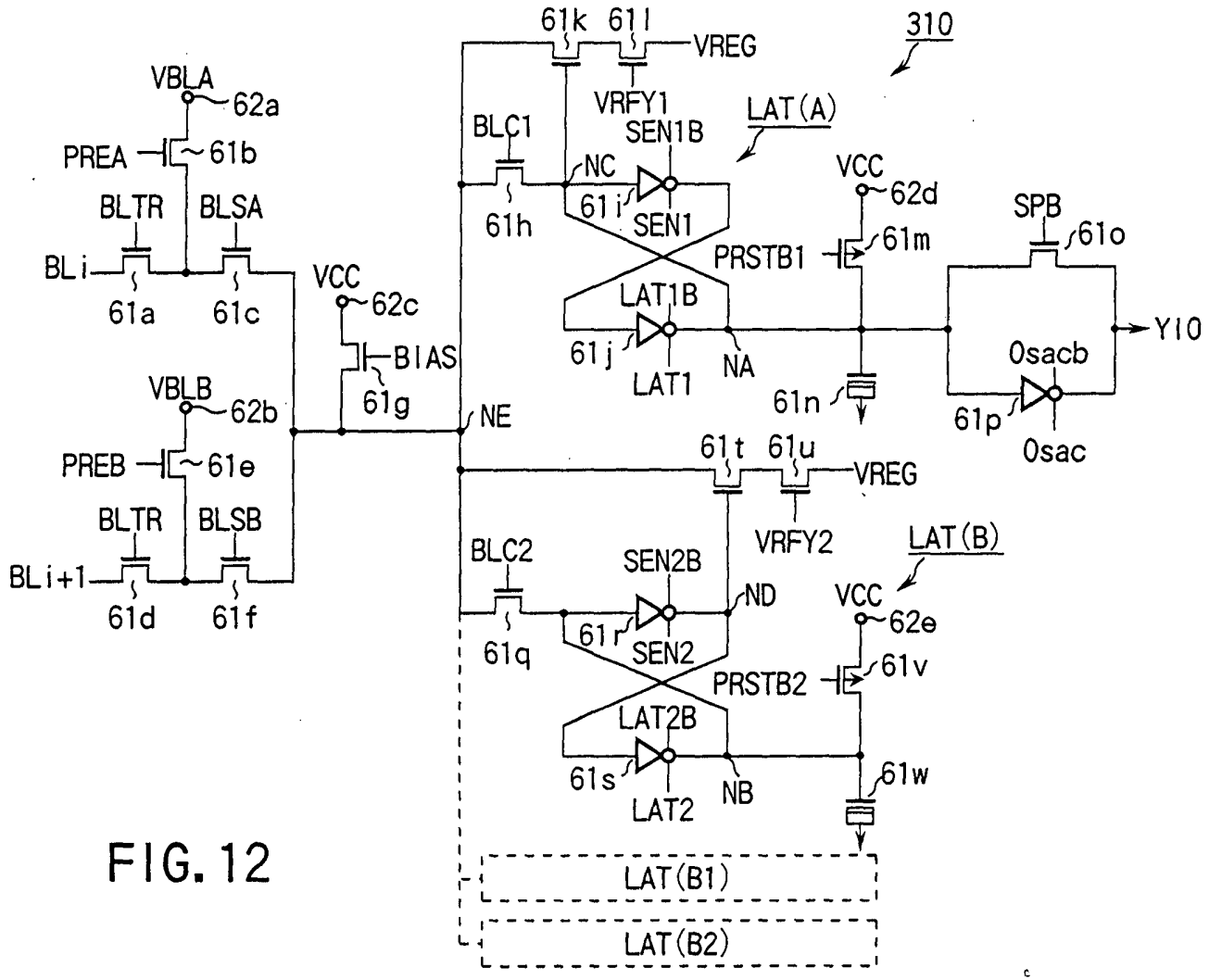
61k
61l
VREG
310
VBLA
62a
VRFY1
LAT(A)
PREA
61b
BLC1
SEN1B
BLTR
BLSA
NC
VCC
62d
BLi
61i
SEN1
SPB
61o
61h
PRSTB1
61m
VCC
62c
LAT1B
BIAS
61j
LAT1
NA
Osacb
Y10
61a
61c
61g
61n
61p
VBLB
62b
NE
Osac
61t
61u
VREG
PREB
61e
VRFY2
LAT(B)
BLTR
BLSB
BLC2
SEN2B
VCC
BLi+1
ND
62e
61d
61f
61r
61q
SEN2
61v
PRSTB2
LAT2B
61s
LAT2
NB
61w
LAT(B1)
LAT(B2)

FIG. 12

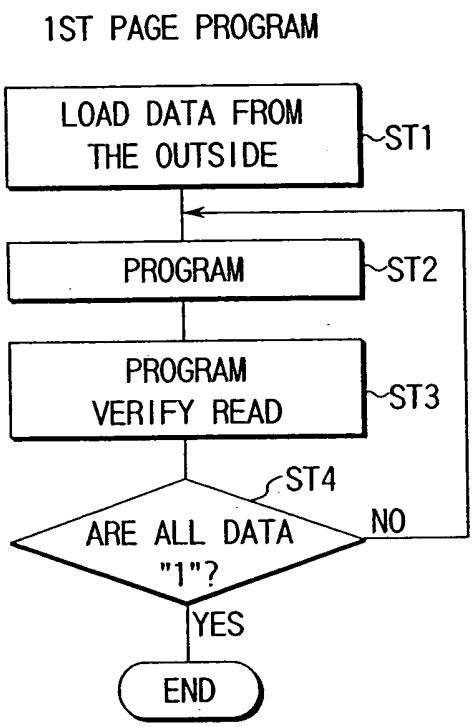

FIG. 13A

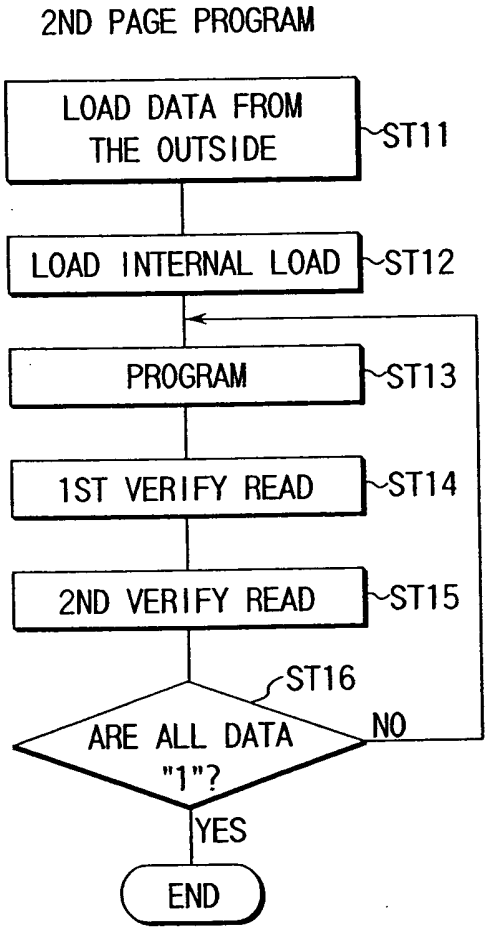

FIG. 13B

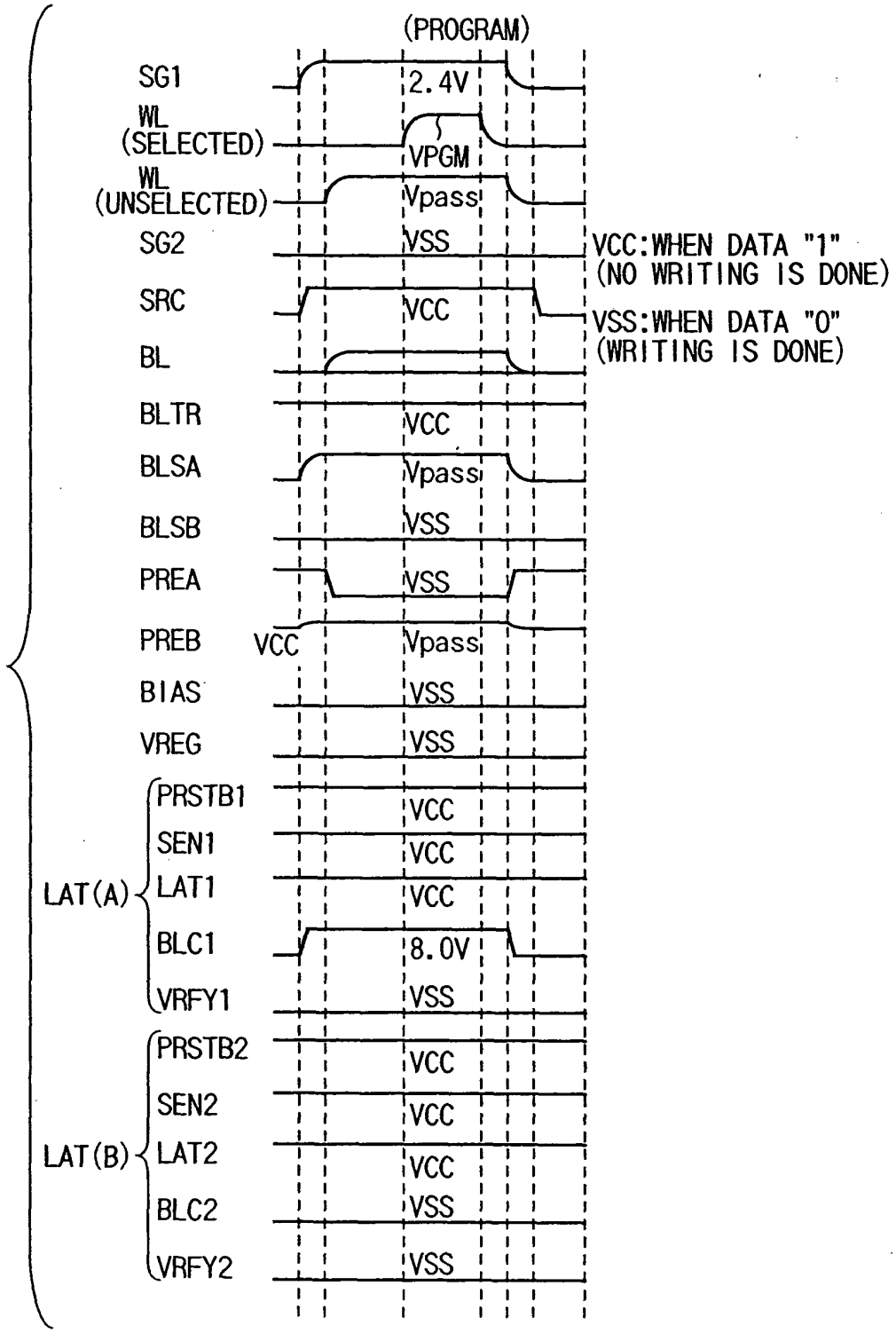
(PROGRAM)
SG1
2.4V
WL
(SELECTED)
VPGM
WL
(UNSELECTED)
Vpass
SG2
VSS
VCC:WHEN DATA "1"
(NO WRITING IS DONE)
SRC
VCC
VSS:WHEN DATA "0"
(WRITING IS DONE)
BL
BLTR
VCC
BLSA
Vpass
BLSB
VSS
PREA
VSS
PREB
VCC
Vpass
BIAS
VSS
VREG
VSS
LAT(A)
PRSTB1
VCC
SEN1
VCC
LAT1
VCC
BLC1
8.0V
VRFY1
VSS
LAT(B)
PRSTB2
VCC
SEN2
VCC
LAT2
VCC
BLC2
VSS
VRFY2
VSS

FIG. 14

PROGRAM VERIFY (1ST PAGE)

STATE 0	STATE 0→1		DATA IN MEMORY CELL	
inhibit A B bit	Write(OK) A B bit	Write(NG) A B bit		
H	L	L	LOAD DATA (write→L, inhibit→H IN A)	
H L	L H	L L	READ AT b'	0→1
H H	L H	L L	MAKE BIT LINE H WHEN A IS H (VERIFY 1)	Verify
H H	H H	L L	LATCH POTENTIAL ON BIT LINE IN A	

(inhibit=NO WRITING, Write=WRITING, A=LAT(A), B=LAT(B))

FIG. 15

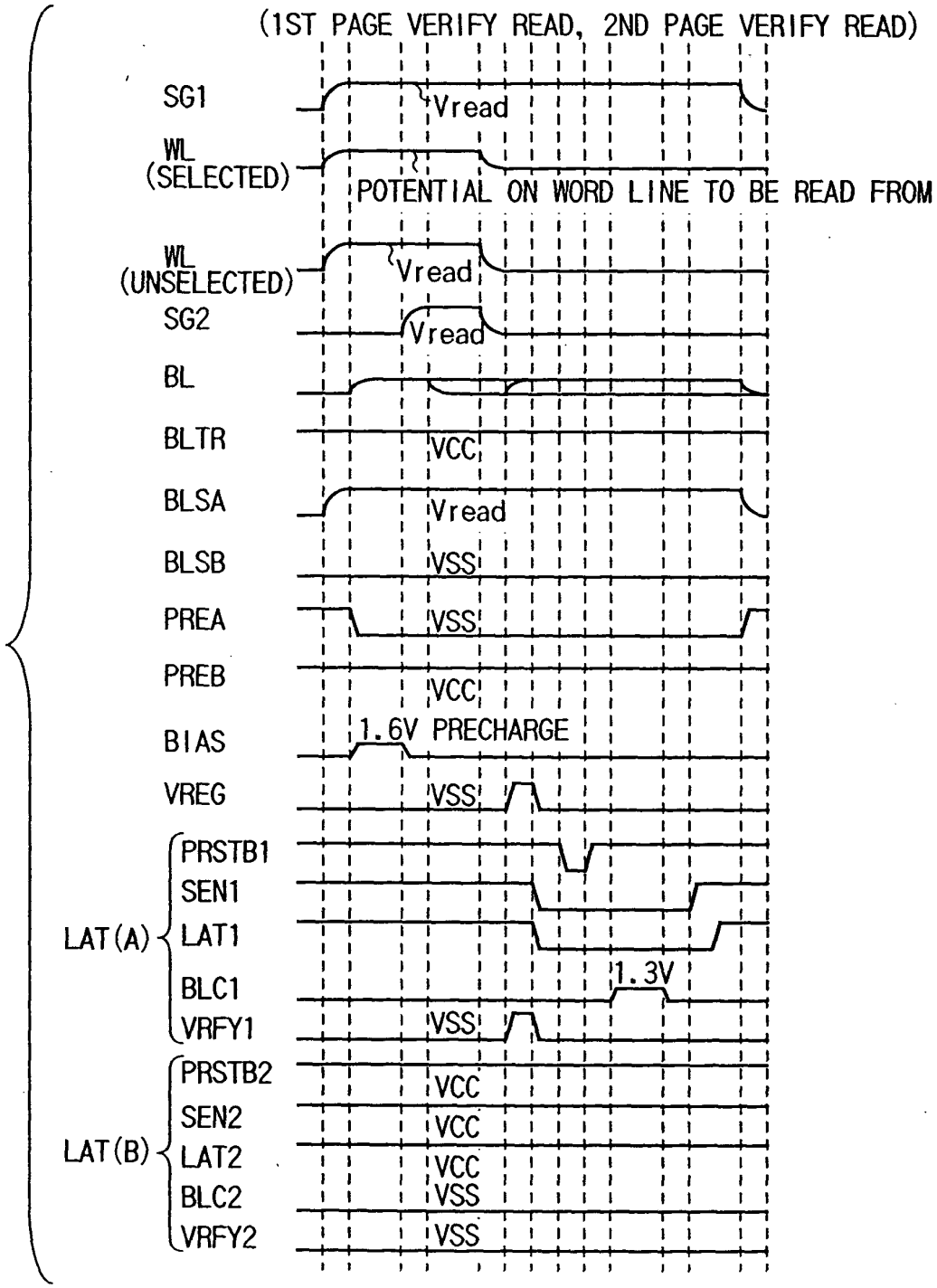
(1ST PAGE VERIFY READ, 2ND PAGE VERIFY READ)
SG1
Vread
WL (SELECTED)
POTENTIAL ON WORD LINE TO BE READ FROM
WL (UNSELECTED)
Vread
SG2
Vread
BL
BLTR
VCC
BLSA
Vread
BLSB
VSS
PREA
VSS
PREB
VCC
BIAS
1.6V PRECHARGE
VREG
VSS
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
1.3V
VRFY1
VSS
LAT(B)
PRSTB2
VCC
SEN2
VCC
LAT2
VCC
BLC2
VSS
VRFY2
VSS

FIG. 16

FIG. 17A

PROGRAM VERIFY (2ND PAGE)

STATE0	STATE0→3		STATE1	STATE1→2		DATA IN MEMORY CELL	
inhibit A B bit	Write(OK) A B bit	Write(NG) A B bit	inhibit A B bit	Write(OK) A B bit	Write(NG) A B bit		
H	L		H	L	L	LOAD DATA (write→L, inhibit→H IN A)	LOAD EXTERNAL DATA
H L H L L	L L L L L		H H H H H	L H L H H		READ AT a LATCH POTENTIAL ON BIT LINE IN B	LOAD INTERNAL DATA

FIG. 17B

H L	L L		H H	L H	L H		
H L L	L L L/H		H H L	L H H	L H L	READ AT b'	1→2
H L L	L L L		H H L	L H H	L H L	MAKE BIT LINE L WHEN B IS L (VRFY2)	Verify
H L H	L L L		H H H	L H H	L H L	MAKE BIT LINE H WHEN A IS H (VRFY1)	
H L H	L L L		H H H	H H H	L H L	LATCH POTENTIAL ON BIT LINE IN A	

FIG. 17C

H L	L L	L L	H H	L H			
H L L	L L H	L L L	H H L	L H L		READ AT b'	3
H L H	L L H	L L L	H H H	L H L		MAKE BIT LINE H WHEN A IS H (VRFY1)	Verify
H L H	H L H	L L L	H H H	L H L		LATCH POTENTIAL ON BIT LINE IN A	

(inhibit=NO WRITING, Write=WRITING, A=LAT(A), B=LAT(B))

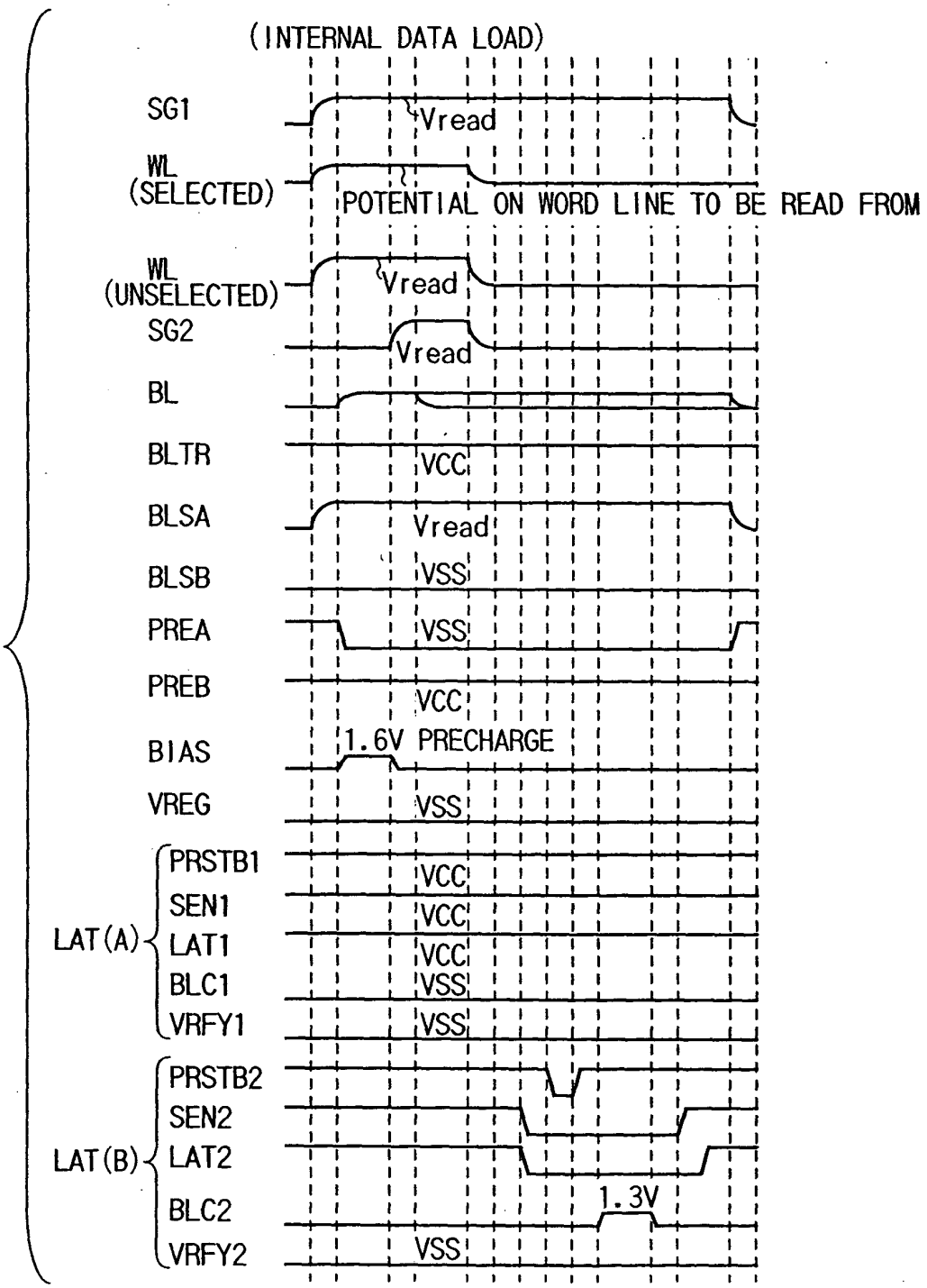
(INTERNAL DATA LOAD)
SG1
Vread
WL
(SELECTED)
POTENTIAL ON WORD LINE TO BE READ FROM
WL
(UNSELECTED)
Vread
SG2
Vread
BL
BLTR
VCC
BLSA
Vread
BLSB
VSS
PREA
VSS
PREB
VCC
BIAS
1.6V PRECHARGE
VREG
VSS
LAT(A)
PRSTB1
VCC
SEN1
VCC
LAT1
VCC
BLC1
VSS
VRFY1
VSS
LAT(B)
PRSTB2
SEN2
LAT2
BLC2
1.3V
VRFY2
VSS

FIG. 18

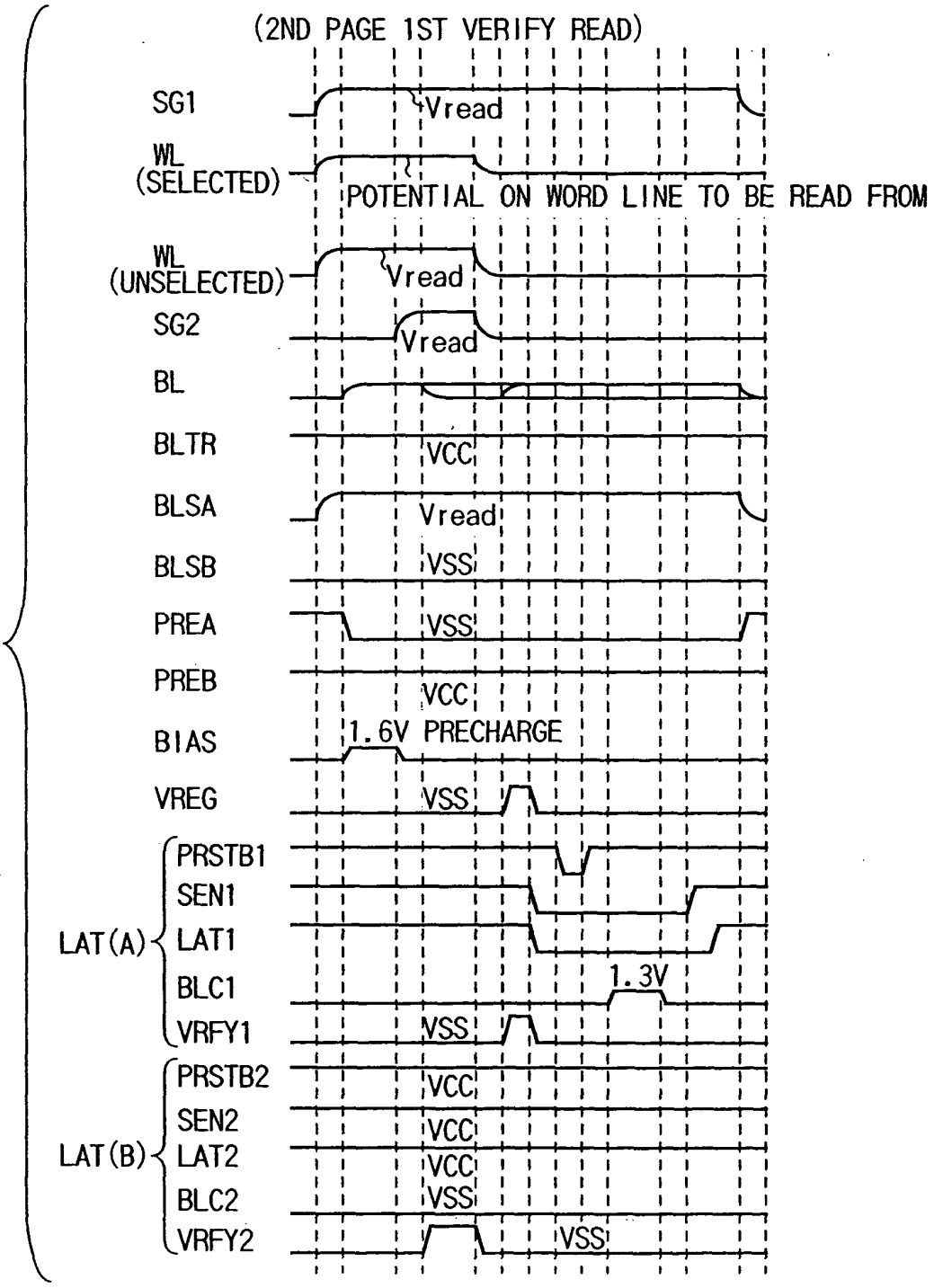
(2ND PAGE 1ST VERIFY READ)
SG1
Vread
WL (SELECTED)
POTENTIAL ON WORD LINE TO BE READ FROM
WL (UNSELECTED)
Vread
SG2
Vread
BL
BLTR
VCC
BLSA
Vread
BLSB
VSS
PREA
VSS
PREB
VCC
BIAS
1.6V PRECHARGE
VREG
VSS
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
1.3V
VRFY1
VSS
LAT(B)
PRSTB2
VCC
SEN2
VCC
LAT2
VCC
BLC2
VSS
VRFY2
VSS

FIG. 19

FIG. 20

READ (2ND PAGE)

STATE0, 1			STATE2, 3				
A	B	bit	A	B	bit		
	L			L		READ AT b	2ND PAGE READ
L	L		L	L		LATCH POTENTIAL ON BIT LINE IN A	

(A=LAT(A), B=LAT(B))

FIG. 21A

READ (1ST PAGE)

STATE0			STATE1, 2			STATE3				
A	B	bit	A	B	bit	A	B	bit		
	L			L			H		READ AT c	1ST READ
L	L		L	L		H	H		LATCH POTENTIAL ON BIT LINE IN LAT(A)	

FIG. 21B

L	L	L	H		H	READ AT a	2ND READ
L	L	L	H	H	L	IF LAT(A) IS H, MAKE BIT LINE L (VRFY1)	
L	L	H	H	L	L	LATCH POTENTIAL ON BIT LINE IN A	

(A=LAT(A), B=LAT(B))

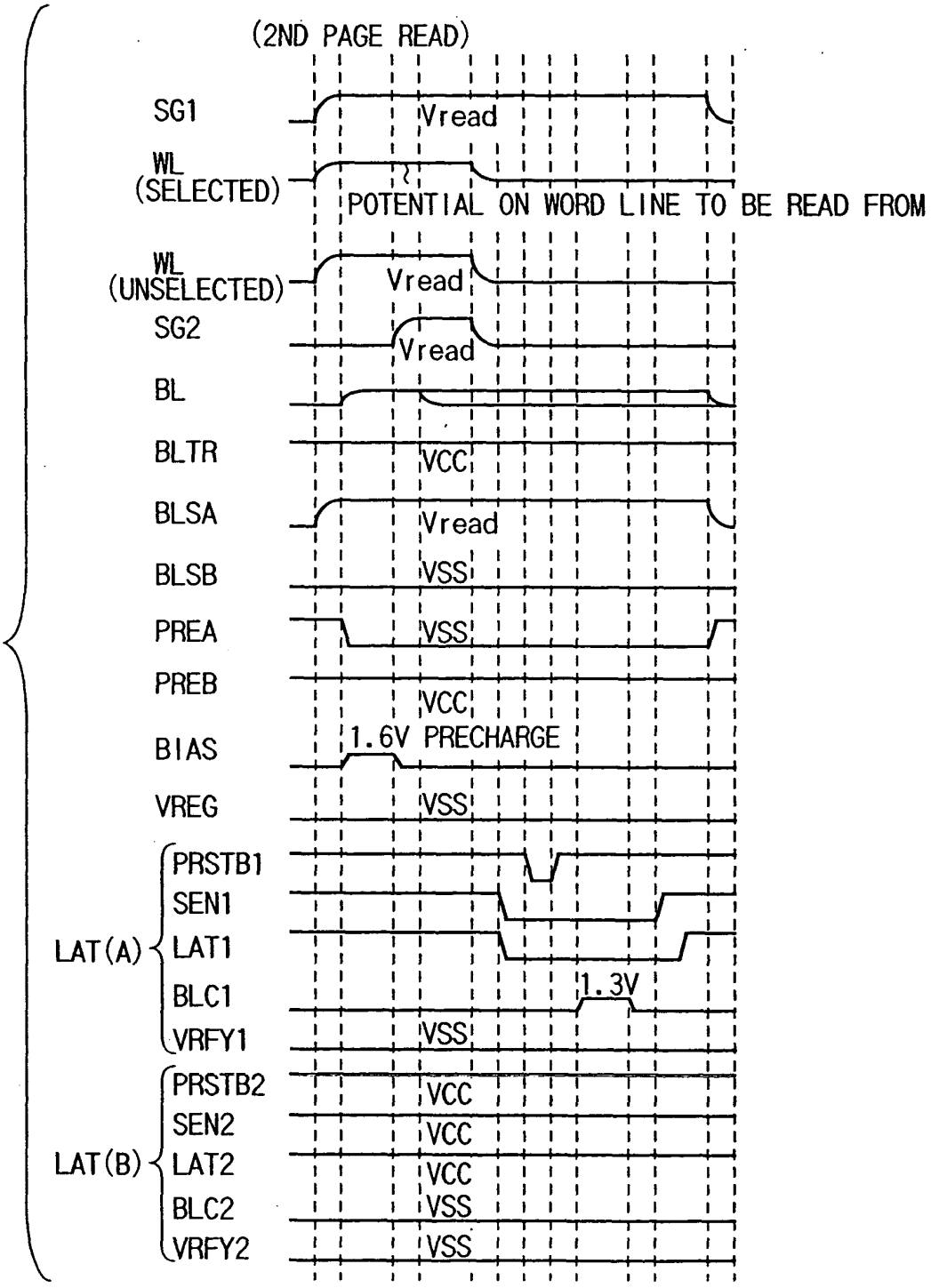
(2ND PAGE READ)
SG1
Vread
WL (SELECTED)
POTENTIAL ON WORD LINE TO BE READ FROM
WL (UNSELECTED)
Vread
SG2
Vread
BL
BLTR
VCC
BLSA
Vread
BLSB
VSS
PREA
VSS
PREB
VCC
BIAS
1.6V PRECHARGE
VREG
VSS
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
1.3V
VRFY1
VSS
LAT(B)
PRSTB2
VCC
SEN2
VCC
LAT2
VCC
BLC2
VSS
VRFY2
VSS

FIG. 22

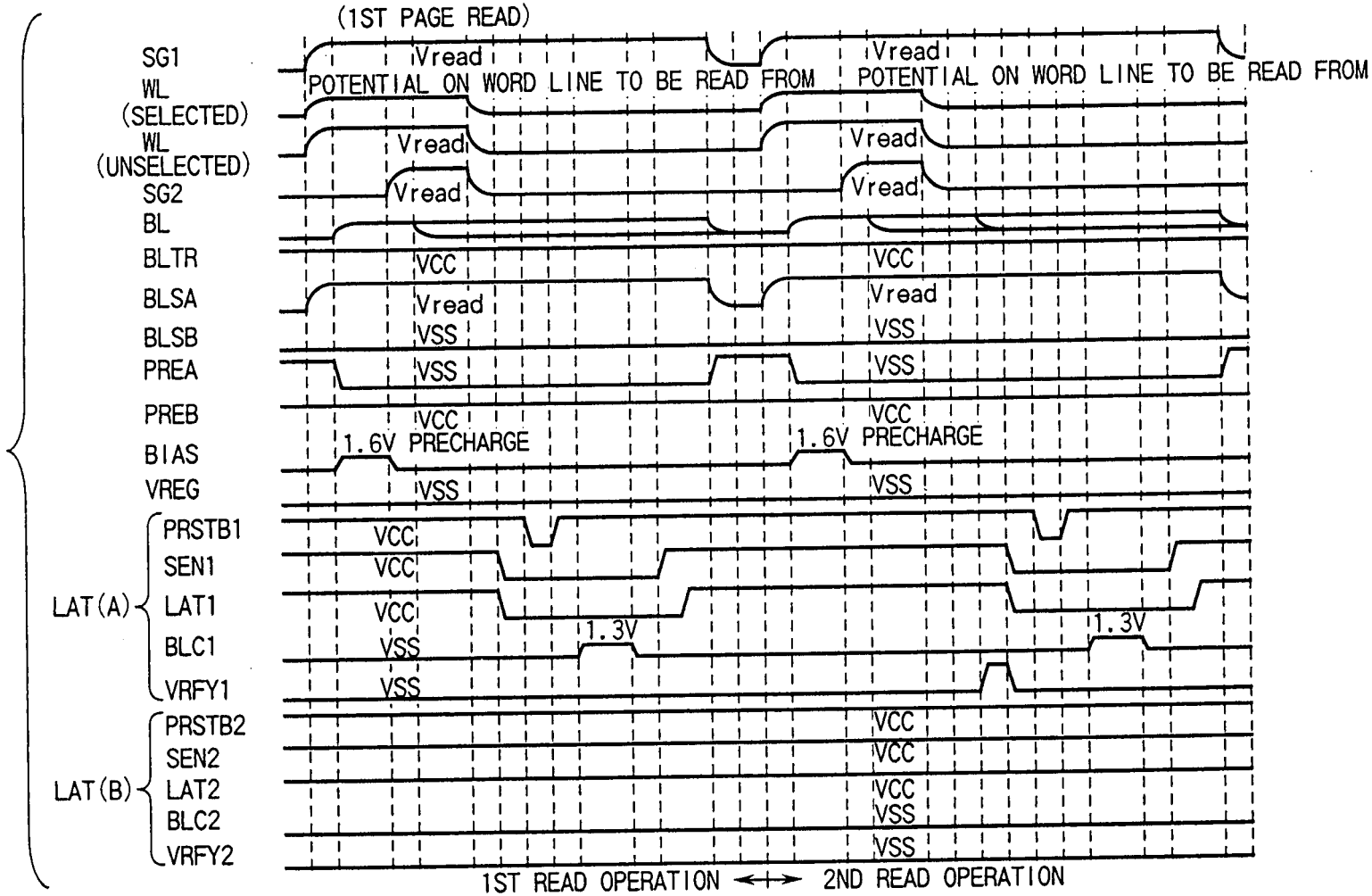
(1ST PAGE READ)
SG1
WL (SELECTED)
WL (UNSELECTED)
SG2
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
VRFY1
LAT(B)
PRSTB2
SEN2
LAT2
BLC2
VRFY2
Vread
POTENTIAL ON WORD LINE TO BE READ FROM
VCC
VSS
1.6V PRECHARGE
1.3V
1ST READ OPERATION
2ND READ OPERATION

FIG. 23

DATA (STATE) IN MEMORY CELL	THRESHOLD VOLTAGE OF MEMORY CELL	DATA TO BE WRITTEN AND READ		
		3RD PAGE	2ND PAGE	1ST PAGE
0	0V OR BELOW	1	1	1
1	0.2V~0.4V	1	1	0
2	0.5V~0.7V	1	0	0
3	0.8V~1.0V	1	0	1
4	1.1V~1.3V	0	0	1
5	1.4V~1.6V	0	0	0
6	1.7V~1.9V	0	1	0
7	2.0V~2.2V	0	1	1

FIG. 24

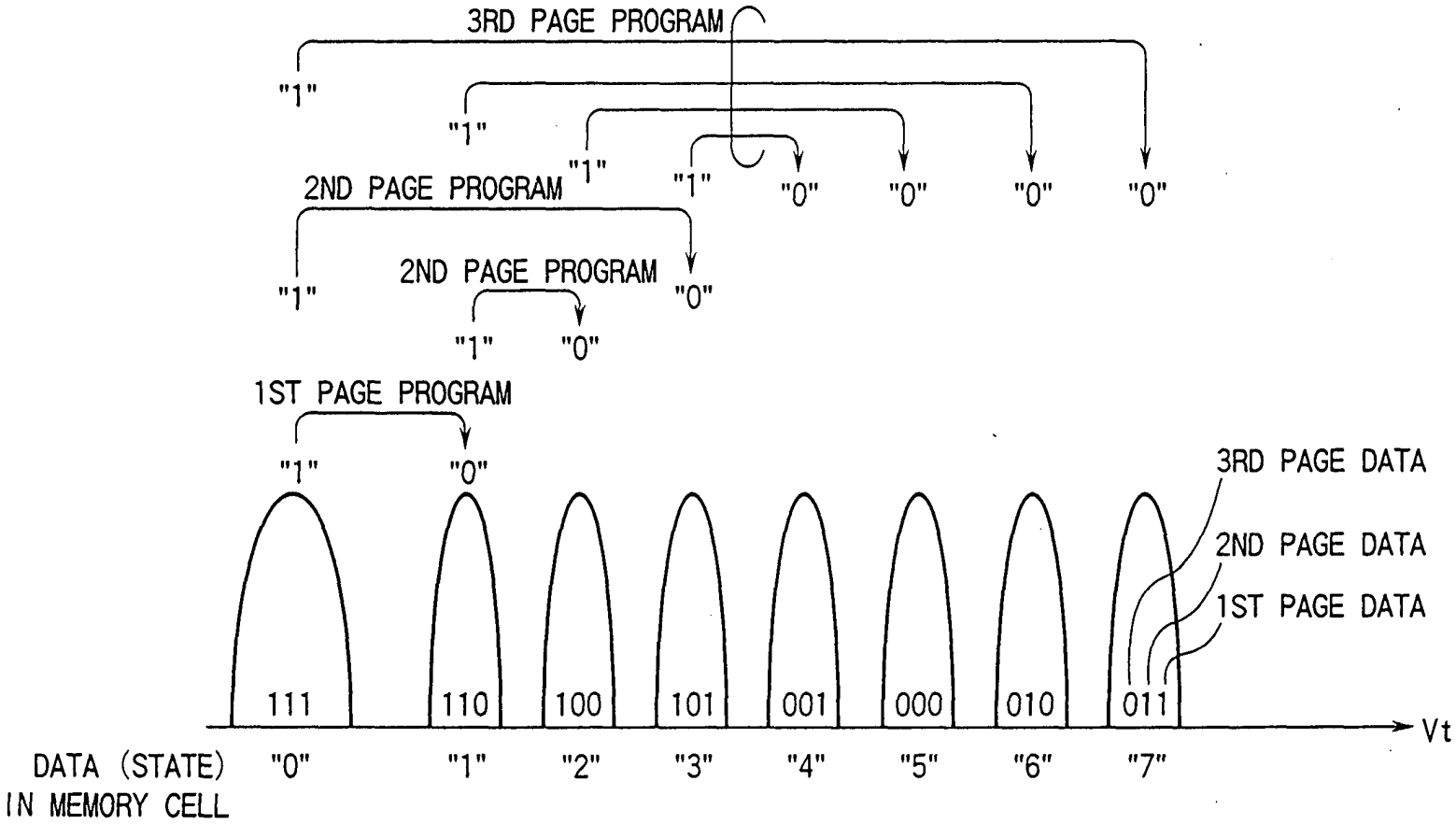
3RD PAGE PROGRAM
"1"
"1"
"1"
"1"
"0"
"0"
"0"
"0"
2ND PAGE PROGRAM
"1"
2ND PAGE PROGRAM
"0"
"1"
"0"
1ST PAGE PROGRAM
"1"
"0"
3RD PAGE DATA
2ND PAGE DATA
1ST PAGE DATA
111
110
100
101
001
000
010
011
Vt
DATA (STATE) IN MEMORY CELL
"0"
"1"
"2"
"3"
"4"
"5"
"6"
"7"

FIG. 25

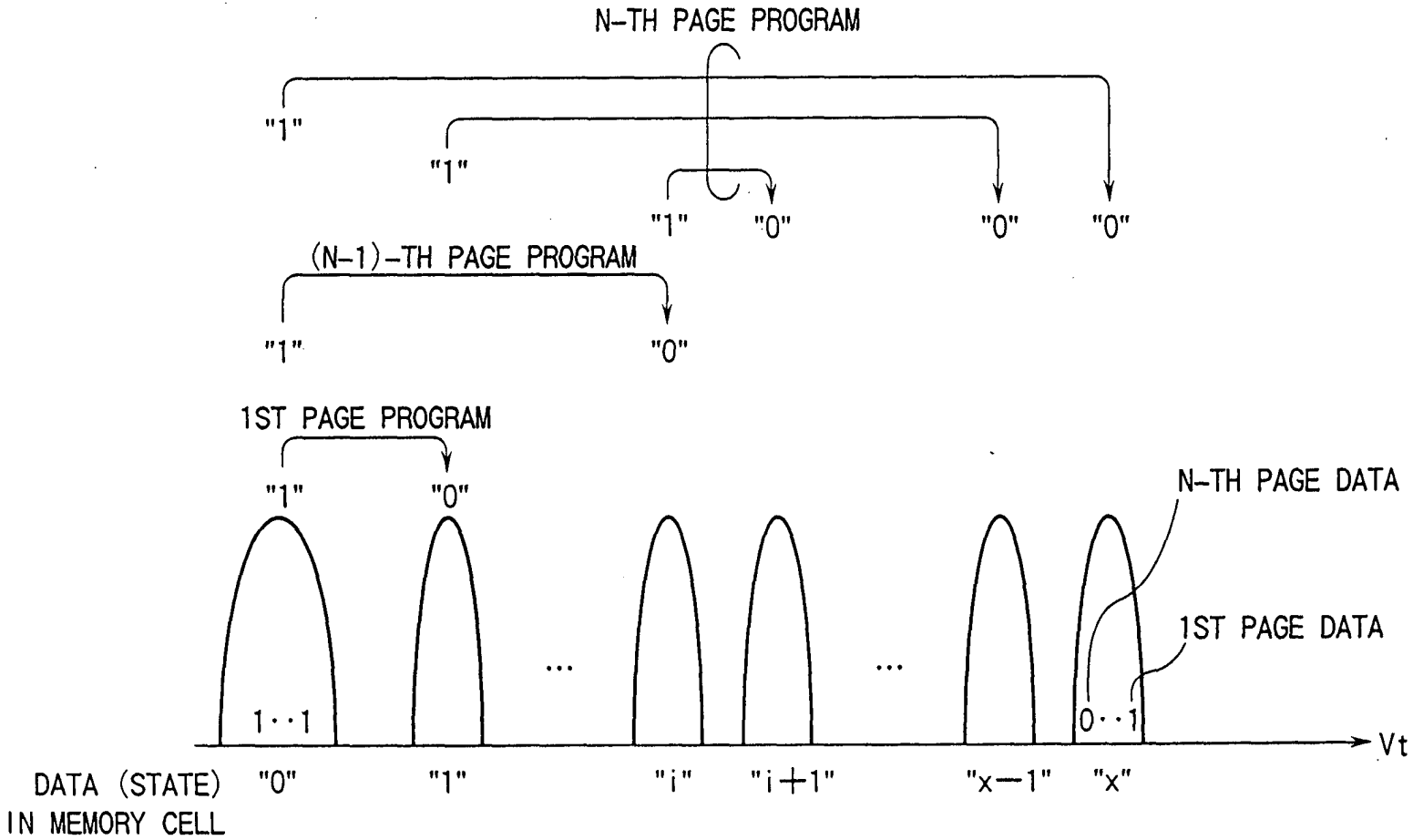
N-TH PAGE PROGRAM
"1"
"1"
"1"
"0"
"0"
"0"
(N-1)-TH PAGE PROGRAM
"1"
"0"
1ST PAGE PROGRAM
"1"
"0"
N-TH PAGE DATA
1ST PAGE DATA
1··1
0··1
Vt
DATA (STATE)
IN MEMORY CELL
"0"
"1"
"i"
"i+1"
"x-1"
"x"

FIG. 26